

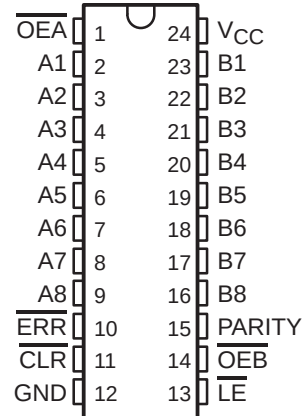
SN74ALS29854

8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SDAS118C – FEBRUARY 1987 – REVISED JANUARY 1995

- Functionally Similar to AMD's AM29854
- High-Speed Bus Transceiver With Parity Generator/Checker
- Parity-Error Flag With Open-Collector Outputs
- Latch for Storing the Parity-Error Flag
- Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic (NT) 300-mil DIPs

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74ALS29854 is an 8-bit to 9-bit parity transceiver designed for two-way communication between data buses. When data is transmitted from the A bus to the B bus, a parity bit is generated. When data is transmitted from the B bus to the A bus with its corresponding parity bit, the parity-error ($\overline{\text{ERR}}$) output indicates whether or not an error in the B data has occurred. The output-enable ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector $\overline{\text{ERR}}$ flag. $\overline{\text{ERR}}$ can be either passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{\text{LE}}$) and clear ($\overline{\text{CLR}}$) control inputs. When both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition that gives the designer more system diagnostic capability.

The SN74ALS29854 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS						OUTPUT AND I/O				OPERATION
$\overline{\text{OEB}}$	$\overline{\text{OEA}}$	$\overline{\text{CLR}}$	$\overline{\text{LE}}$	Ai Σ of Hs	Bi [†] Σ of Ls	A	B	PARITY	$\overline{\text{ERR}}^{\ddagger}$	
L	H	X	X	Odd Even	NA	NA	$\overline{\text{A}}$	H L	NA	$\overline{\text{A}}$ data to B bus and generate parity
H	L	X	L	NA	Odd Even	$\overline{\text{B}}$	NA	NA	H L	$\overline{\text{B}}$ data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	H	H	X	X	Z	Z	Z	NC	Isolation [§]
		L	H	X					H	
		X	L	L Odd H Even					L H	
L	L	X	X	Odd Even	NA	NA	$\overline{\text{A}}$	L H	NA	$\overline{\text{A}}$ data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

[†] Summation of high-level inputs includes PARITY along with Bi inputs.

[‡] Output states shown assume $\overline{\text{ERR}}$ was previously high.

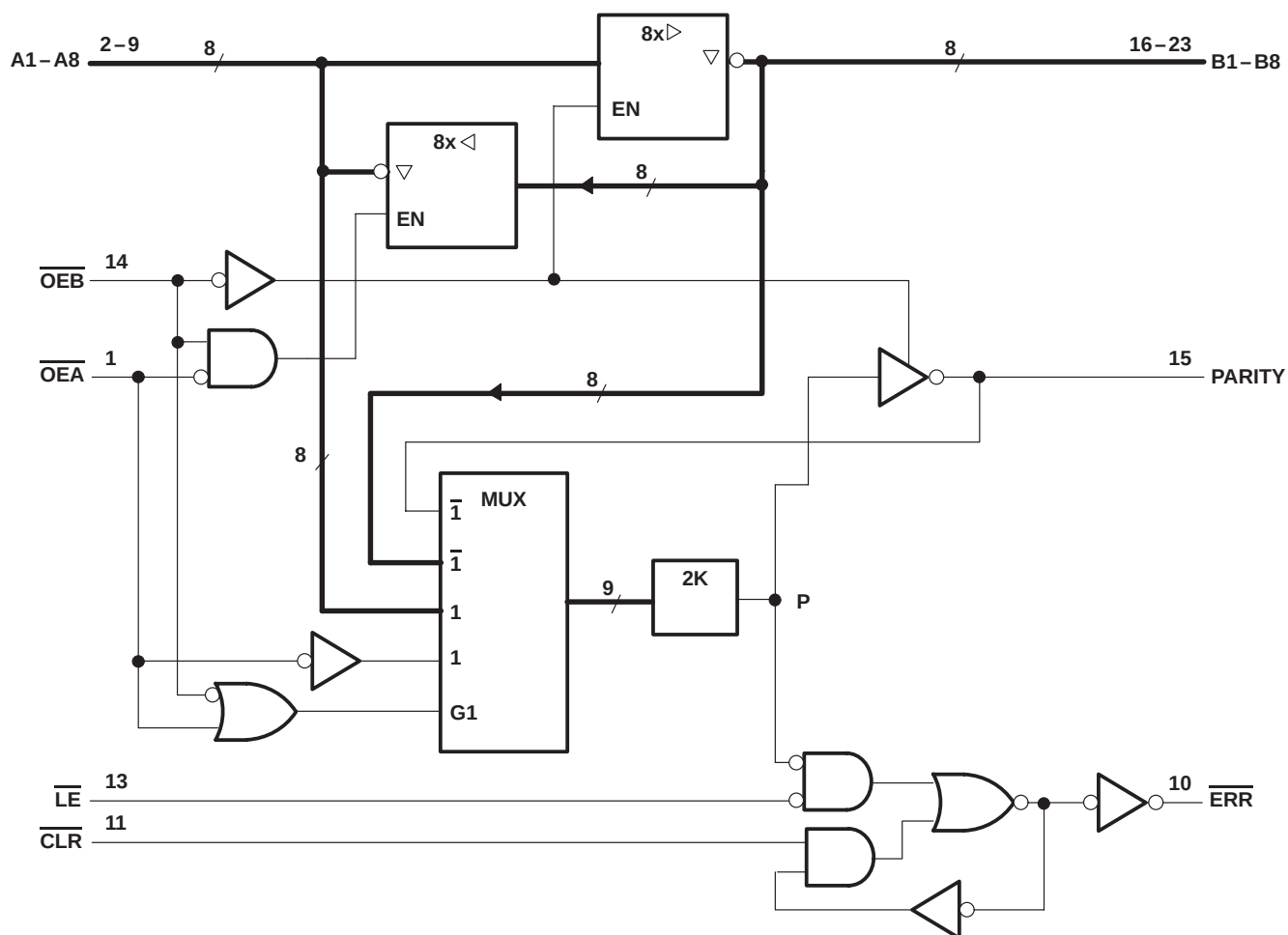
[§] In this mode, $\overline{\text{ERR}}$, when enabled, shows inverted parity of the A bus.

SN74ALS29854

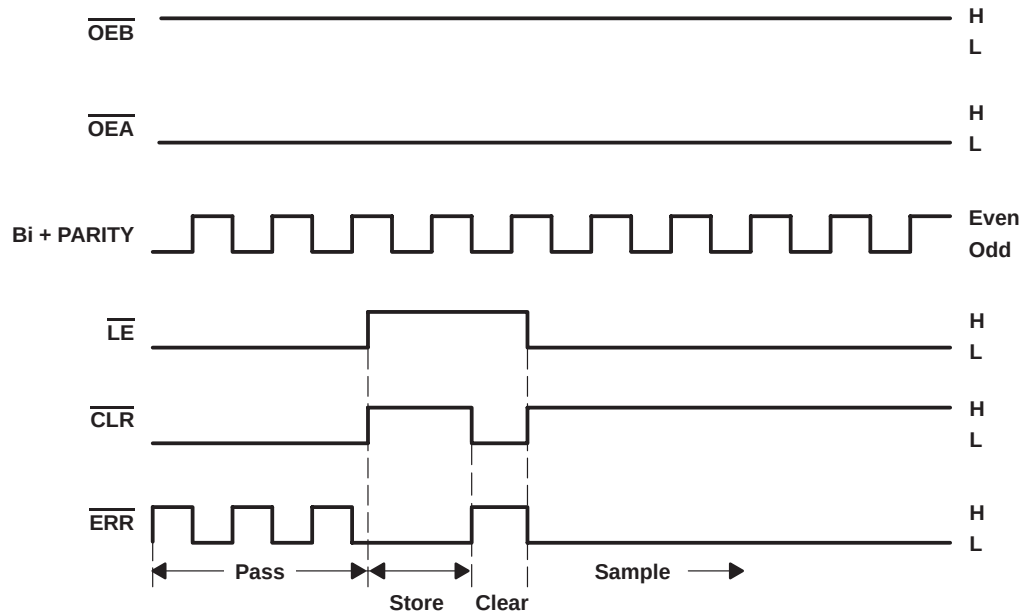
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SDAS118C – FEBRUARY 1987 – REVISED JANUARY 1995

logic diagram (positive logic)



error-flag waveforms



ERROR-FLAG FUNCTIONS

INPUTS		INTERNAL TO DEVICE	OUTPUT PRESTATE	OUTPUT	FUNCTION
$\overline{LE}$	$\overline{CLR}$	POINT P	$\overline{ERR}_{n-1}^\dagger$	$\overline{ERR}$	
L	L	L H	X	L H	Pass
L	H	L X H	X L H	L L H	Sample
H	L	X	X	H	Clear
H	H	X	L H	L H	Store

$^\dagger \overline{ERR}_{n-1}$ represents the state of ERR before any changes at CLR, LE, or point P.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage, V_{CC}	7 V
Input voltage, V_I	7 V
Voltage applied to a disabled I/O port	5.5 V
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range	–65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

SN74ALS29854

8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SDAS118C – FEBRUARY 1987 – REVISED JANUARY 1995

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_{OH}	High-level output voltage, $\overline{ERR}$			5.5	V
I_{OH}	High-level output current			–24	mA
I_{OL}	Low-level output current			48	mA
t_w	Pulse duration	$\overline{LE}$ high	10		ns
		$\overline{LE}$ low	10		
		CLR low	10		
t_{su}	Setup time before $\overline{LE}\downarrow$	Bi and PARITY	10		ns
		CLR high	15		
t_h	Hold time, Bi and PARITY after $\overline{LE}\downarrow$	3			ns
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IK}		$V_{CC} = 4.75\text{ V}$,	$I_I = -18\text{ mA}$			–1.2	V
V_{OH}	All I/Os except $\overline{ERR}$	$V_{CC} = 4.75\text{ V}$	$I_{OH} = -15\text{ mA}$	2.4			V
			$I_{OH} = -24\text{ mA}$	2			
I_{OH}	$\overline{ERR}$	$V_{CC} = 4.75\text{ V}$,	$V_{OH} = 5.5\text{ V}$			0.1	mA
V_{OL}		$V_{CC} = 4.75\text{ V}$,	$I_{OL} = 48\text{ mA}$	0.35	0.5		V
I_I		$V_{CC} = 5.25\text{ V}$,	$V_I = 5.5\text{ V}$			0.1	mA
$I_{IH}^{\ddagger}$		$V_{CC} = 5.25\text{ V}$,	$V_I = 2.7\text{ V}$			20	μA
$I_{IL}^{\ddagger}$	Data	$V_{CC} = 5.25\text{ V}$,	$V_I = 0.4\text{ V}$			–0.2	mA
	Control					–0.75	
$I_O^{\S}$		$V_{CC} = 5.25\text{ V}$,	$V_O = 0$	–75		–250	mA
I_{CC}		$V_{CC} = 5.25\text{ V}$,	All outputs open		70	100	mA

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

[§] The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS} .



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	$V_{CC} = 4.75 \text{ V to } 5.25 \text{ V}$, $T_A = \text{MIN to MAX}^\dagger$		UNIT
				MIN	MAX	
t_{PLH}	A or B	B or A	$C_L = 50 \text{ pF}$		8	ns
t_{PHL}					8	
t_{PLH}	A or B	B or A	$C_L = 300 \text{ pF}$		13	ns
t_{PHL}					13	
t_{PLH}	A	PARITY	$C_L = 50 \text{ pF}$		15	ns
t_{PHL}					18	
t_{PLH}	A	PARITY	$C_L = 300 \text{ pF}$		22	ns
t_{PHL}					22	
t_{PZH}	$\overline{OE}A$ or $\overline{OE}B$	A or B	$C_L = 50 \text{ pF}$		17	ns
t_{PZL}					17	
t_{PZH}	$\overline{OE}A$ or $\overline{OE}B$	A or B	$C_L = 300 \text{ pF}$		23	ns
t_{PZL}					23	
t_{PHZ}	$\overline{OE}A$ or $\overline{OE}B$	A or B	$C_L = 5 \text{ pF}$		8	ns
t_{PLZ}					8	
t_{PHZ}	$\overline{OE}A$ or $\overline{OE}B$	A or B	$C_L = 50 \text{ pF}$		15	ns
t_{PLZ}					8	
t_{PHL}	$\overline{LE}$	$\overline{ERR}$	$C_L = 50 \text{ pF}$		12	ns
t_{PLH}	$\overline{CLR}$	$\overline{ERR}$	$C_L = 50 \text{ pF}$		12	ns
t_{PLH}	$\overline{OE}A$	PARITY	$C_L = 50 \text{ pF}$		17	ns
t_{PHL}					19	
t_{PLH}	$\overline{OE}A$	PARITY	$C_L = 300 \text{ pF}$		22	ns
t_{PHL}					25	
t_{PLH}	Bi/PARITY	$\overline{ERR}$	$C_L = 50 \text{ pF}$		20	ns
t_{PHL}					20	

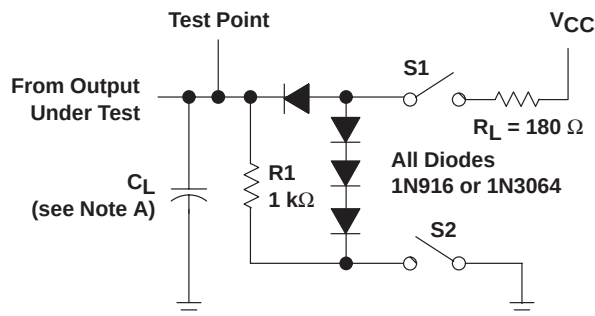
[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

SN74ALS29854

8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

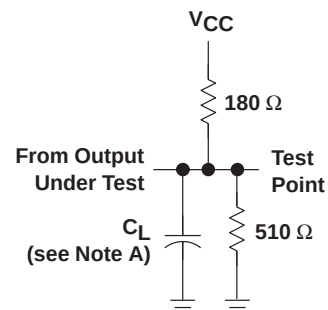
SDAS118C – FEBRUARY 1987 – REVISED JANUARY 1995

PARAMETER MEASUREMENT INFORMATION

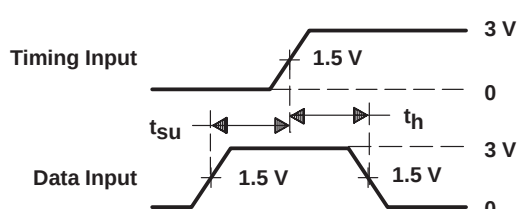


LOAD CIRCUIT 1
ALL OUTPUTS EXCEPT FOR ERROR FLAG

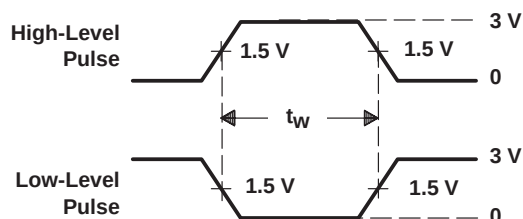
SWITCH POSITION TABLE		
TEST	S1	S2
t_{PLH}	Closed	Closed
t_{PHL}	Closed	Closed
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PHZ}	Closed	Closed
t_{PLZ}	Closed	Closed



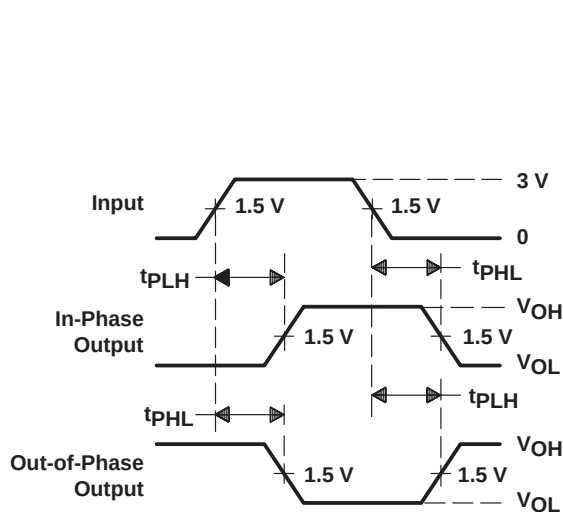
LOAD CIRCUIT 2
ERROR-FLAG OUTPUT



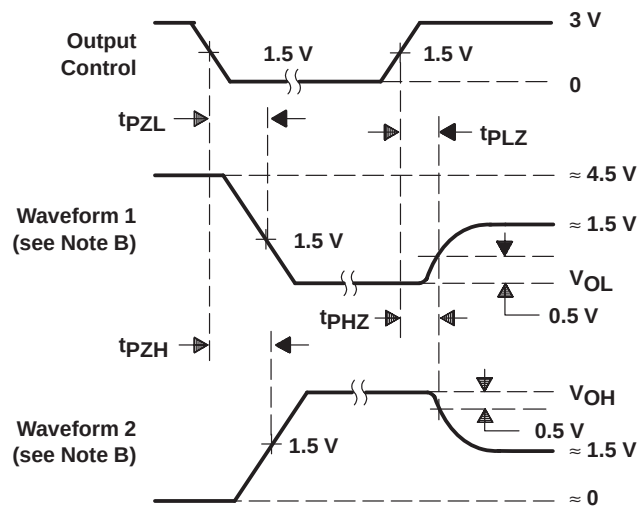
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS29854DW	ACTIVE	SOIC	DW	24	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS29854DWR	ACTIVE	SOIC	DW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
SN74ALS29854NT	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74ALS29854NT3	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

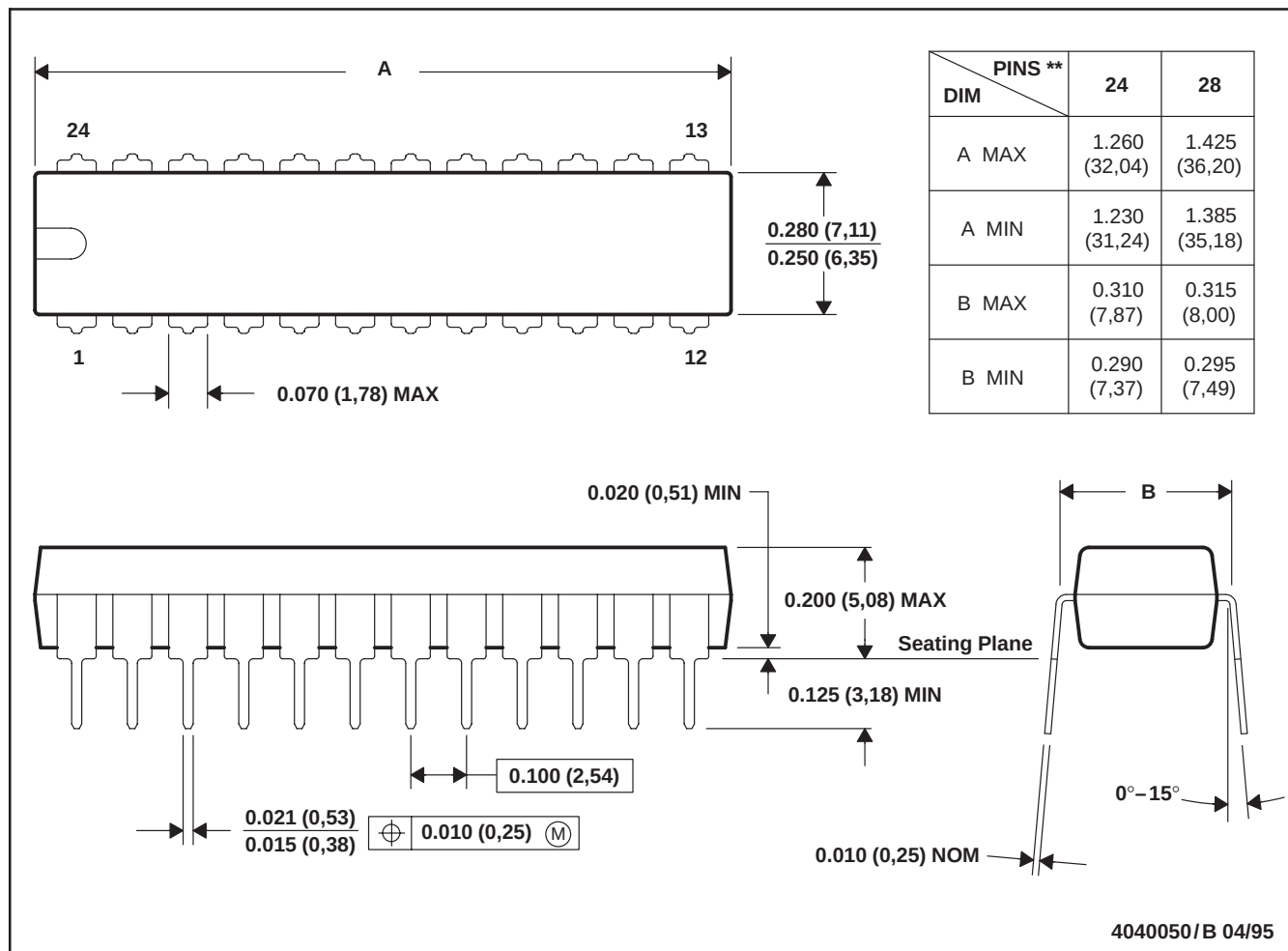
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

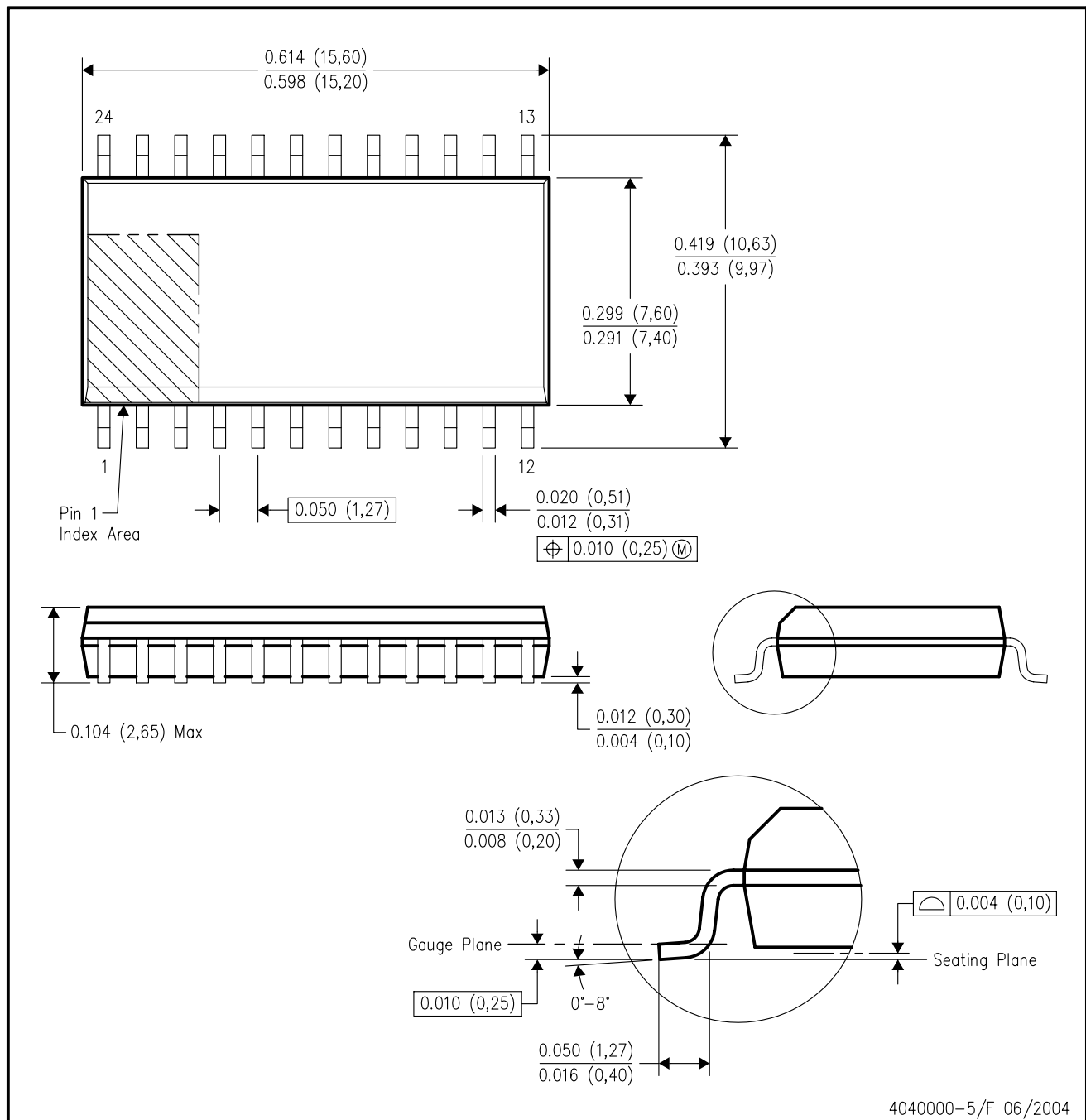
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated